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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,028	01/31/2002	Peter T. Liu	37310-000137	2099
30595	7590	06/13/2003		
HARNESS, DICKEY & PIERCE, P.L.C. P.O. BOX 8910 RESTON, VA 20195			EXAMINER TRA, ANH QUAN	
			ART UNIT 2816	PAPER NUMBER

DATE MAILED: 06/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/066,028	LIU, PETER T.
	Examiner Quan Tra	Art Unit 2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 21 April 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-5 and 7-16 is/are rejected.

7) Claim(s) 6 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ .
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. .	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

This office action is in response to the amendment filed 04/21/2003. The rejections in previous are maintained.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 8-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 is misdescriptive and renders the claim indefinite. It is misdescriptive for reciting “a validation circuit dynamically adjusting a validation point of the sense amplifier base on operating conditions...”. It is not clear how the validation circuit “dynamically adjusting a validation point of the sense amplifier” since the output of the validation circuit is not coupled to control the sense amplifier. Figure 1 shows the validation circuit (70) has no relationship with the sense amplifier (50). The INVALID signal is for indicating the state of the power down signal (PDN). For example, when signal PDN is low, the INVALID signal is high, and when the PDN signal is low, the INVALID signal is high.

Claims 8-13 are rejected as including the indefiniteness of claim 8.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 8-11 and 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Starnes et al. (USP 6157583).

As to claims 1, 8, and 14, Starnes et al. discloses in figure 2 a buried fuse reading device, comprising: at least one buried fuse (208), at least one sense amplifier (202) sensing a condition of the buried fuse; and a validation circuit (258 in 206) detecting and indicating when output from the sense amplifier is valid. As further called in for claim 14, the inverter 258 tracks operation of the sense amplifier such that the inverter 258 indicates when the sense amplifier has sufficiently settled on sense condition of the buried fuse (when the inverter 258 at high impedance state, it is indicated that circuits 202 and 204 are disabled).

As to claim 2, figure 2 shows the validation circuit detects when the sense amplifier has sufficiently settled on a sensed condition of the buried fuse.

As to claim 3, 9 and 15, figures 1-3 further shows a power control circuit (118 and 120 in figure 1, and 120 in figure 3) for powering the buried fuse reading device up and down; and wherein the validation circuit detects when the sense amplifier has sufficiently settled on a sensed condition once the power control circuit begins powering up the buried fuse reading device.

As to claims 4, 10, it is inherent for the circuit of figure 2 to have a bias generating circuit for generating first (Vdd) and second voltages (Vss); and wherein the sense amplifier operates based on the first and second voltages.

As to claims 5, 11, figure 2 shows the validation circuit operates based on the first and second voltages.

As to claim 16, figure 2 shows the sense amplifier (202) and the tracking circuit (258) draw substantially no current when the power control circuit has the buried fuse reading device power down. (when Drive signal is low, transistor 216, 220, 210 are off, and input of 258 is at high impedance state, thus the output of 5 258 is at high impedance state).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Starnes et al. (USP 6157583).

Starnes et al.'s figure 2 shows all limitations of the claims. Figure 2 fails to show plurality of buried fuses. However, it is well known in the art that plurality of fuses connected in parallel will decreasing the resistance of the fuse circuit. Therefore, it would have been obvious to one having ordinary skill in the art to replace fuse 208 with plurality of fuses connected in parallel for the purpose of reducing the resistance of the fuse circuit.

Allowable Subject Matter

7. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claim 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 6 and 12 would be allowable because the prior art fails to teach or suggest a circuit (such as figure 1) having a sense amplifier 50 includes first PMOS transistor (54) and a first NMOS transistor (56) connected in series with the buried metal fuse (52), a gate of the first PMOS transistor receiving the first voltage (BHI) and the gate of the first NMOS transistor receiving the second voltage (BLO); the validation circuit (70) includes a second PMOS transistor (72) and a second NMOS transistor (74) connected in series, a gate of the second PMOS transistor receiving the first voltage and a gate of the second NMOS transistor receiving the second voltage, the second PMOS and NMOS transistor being weaker than the first PMOS and NMOS transistors, respectively.

Response to Arguments

9. Applicant's arguments have been fully considered but they are not persuasive.

In response to the argument under "Rejection Under 35 U.S.C. § 112, Second Paragraph", nowhere in page 8 of the specification that indicated the "validation circuit dynamically adjusting a validation point of the sense amplifier". It is also not seen in the drawing the output of the validation circuit is coupled to the sense amplifier in order to controlling the characteristic of the sense amplifier. Therefore, claims 8-10 are misdescriptive.

In response to the argument under "Rejection Under 35 U.S.C. § 102, claim 1, as broad as reasonable interpretation, "detecting" the validation of the output of the amplifier is seen as detecting the state of the output of the amplifier. And inverter 258 detecting the state of the

amplifier output signal. Furthermore, inverter 258 is at high impedance state when circuits 202 and 204 are disable, thus, indicating the output of the sense amplifier is not valid.

In response to the argument under “Rejection Under 35 U.S.C. § 102, claim 8, it is not seen how the validation circuit can “dynamically adjusting a validation point for a sense amplifier” since the output of the validation circuit is not coupled to control the sense amplifier. Furthermore, “detecting” the validation of the output of the amplifier is seen as detecting the state of the output of the amplifier. And inverters 258 and 260 detecting the state of the amplifier output signal. Furthermore, inverter 258 is at high impedance state when circuits 202 and 204 are disable, thus, indicating the output of the sense amplifier is not valid.

Therefore, insofar as understood, figure 2 meets all limitations of the claim.

In response to the argument under “Rejection Under 35 U.S.C. § 102, claim 14, the inverter 258 tracking the condition of the sense amplifier by indicating the sense amplifier circuit is disabled when the inverter 258 is at high impedance state. Therefore, figure 2 shows all limitations of the claim.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
June 4, 2003


Terry J. Cunningham
Primary Examiner